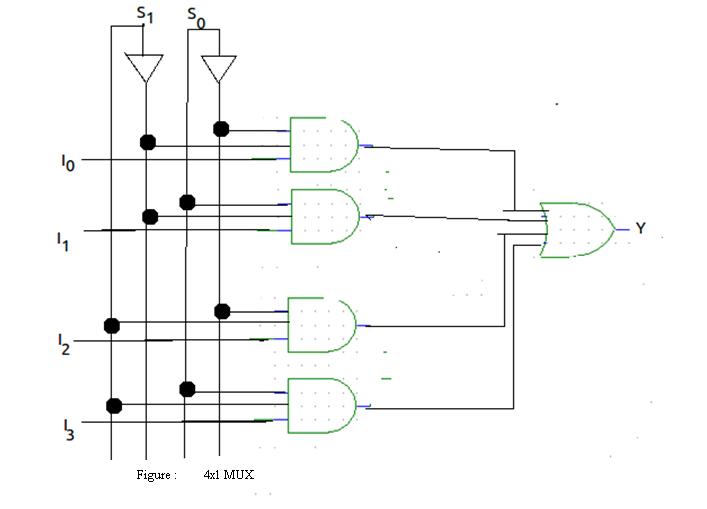
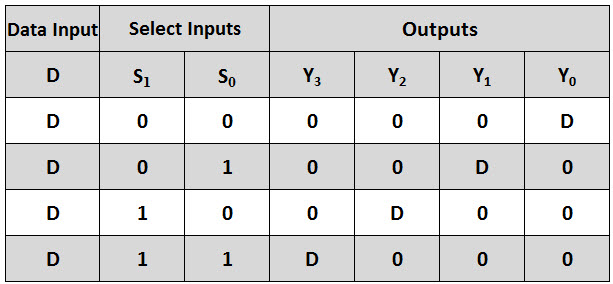
**Circuit Diagram & Truth Table:**

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**Code:**

* **Design Module**

module mux(out,s0,s1,i0,i1,i2,i3);

input s0,s1,i0,i1,i2,i3;

output out;

wire s0n,s1n,a,b,c,d;

not n1(s0n,s0);

not n2(s1n,s1);

and a1(a,s0n,s1n,i0);

and a2(b,s0n,s1,i1);

and a3(c,s0,s1n,i2);

and a4(d,s0,s1,i3);

or o1(out,a,b,c,d);

endmodule

* **TestBench**

module Baig;

reg s0,s1,i0,i1,i2,i3;

wire out;

mux m1(out,s0,s1,i0,i1,i2,i3);

initial

begin

s0=1'b0;s1=1'b0;i0=1'b0;i1=1'b0;i2=1'b0;i3=1'b0;

#20

s0=1'b0;s1=1'b0;i0=1'b0;i1=1'b0;i2=1'b0;i3=1'b1;

#20

s0=1'b0;s1=1'b1;i0=1'b0;i1=1'b0;i2=1'b1;i3=1'b0;

#20

s0=1'b0;s1=1'b1;i0=1'b0;i1=1'b0;i2=1'b1;i3=1'b1;

#20

s0=1'b1;s1=1'b0;i0=1'b0;i1=1'b1;i2=1'b0;i3=1'b0;

#20

s0=1'b1;s1=1'b0;i0=1'b0;i1=1'b1;i2=1'b0;i3=1'b1;

#20

s0=1'b1;s1=1'b1;i0=1'b0;i1=1'b1;i2=1'b1;i3=1'b0;

#20

s0=1'b1;s1=1'b1;i0=1'b0;i1=1'b1;i2=1'b1;i3=1'b1;

#20

$finish;

end

endmodule

**Output:**

Graphical user interface, application, table

Description automatically generated